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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/901,746	07/10/2001	Yoshinori Takahashi	36856.526	8463

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EXAMINER	
NGUYEN, HIEP	
ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 09/25/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/901,746	TAKAHASHI, YOSHINORI	
	Examiner	Art Unit	
	Hiep Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the c rrespondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 August 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Specification

The disclosure is objected to because of the following informalities: element (16) has two different names for instance, in page 6, line 15, element (16) is "a first dielectric layer"; on lines 19-20, element (16) is the "first grounding conductor layer"; on page 8, line 17, element (16) is "the first grounding conductor layer".

Appropriate correction is required.

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the recitation "two conductor layers" in claims 1 and 3 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claim 1 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. In this instance, the specification fails to describe "one of the omitted portions is **aligned** with the through hole and another of the omitted

portions is aligned with the micro strip line". Figure 2 of the present application shows **only one omitted portion** (32) and this omitted portion is **not aligned** with the through hole (30).

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Correction and/or clarification is required.

Regarding claim 1, the recitation "and including at least **two conductor layers** which include at least two grounding conductor layers and a plurality of dielectric layers" on lines 2-4 is indefinite because it is unclear as to how conductor layers can **include** grounding conductor layers and a plurality of dielectric layers". According to figure 2 of the present application, the grounding conductor layers are (14) and (24), the dielectric layers are (16), (22) and (26) and no conductor layers are shown. As understood by the examiner, the multi-layer substrate 12, fig.2, includes at least two grounding conductor layers (3,5,7) and a plurality of dielectric layers (2a-2g) and a plurality of dielectric layers (16, 22, 26). The **two conductor layers** should be excluded from the claim and the "two conductor layer" on line 10 should be --two grounding conductor layer--. The recitation " one of the omitted portions is aligned with the through hole and another of the omitted portions is aligned with the microstrip line" is indefinite because it is misdescriptive. In figure 2 of the present application, there is **only one** omitted portion (32) that is "aligned" with the microstrip line (28). The through hole (30) is not considered to be aligned with the omitted portion (32). It is positioned next to the omitted portion (32). Moreover, figure 2 shows only one omitted portion (32). The same analysis is true for claims 8 and 14.

Regarding claim 2, the recitation "wherein said omitted portion aligned with the microstrip line is arranged such that said grounding conductor layer disposed on the lower surface of said multilayer substrate faces said microstrip line" is indefinite because it does not make sense. Figure 2 only shows that the omitted portion (32) facing the microstrip line (28) is on the grounding conductor layer (24) that is above the other grounding conductor layer (14).

The location of the grounding conductor layer (14) has nothing to do with the omitted portion (32).

Regarding claim 3, the recitation " wherein said omitted portion**s** **define** openings in said one of the at least two conductor layers" is indefinite because it is misdescriptive. Figure 2 of the present application shows that there is **only one** omitted portion (32) and **one opening** defined by said "omitted portion". The "two conductor layers" do not exist in the drawing.

Regarding claims 4 and 18, the recitation "said openings have one of a substantial rectangular shape **and** a substantially square shape " is indefinite because it is misdescriptive. There is only **one** opening in figure 2 and an opening cannot have two different shapes at the same time.

Regarding claim 8, the recitation " one of the openings is aligned with the through hole and another of the openings is aligned with the microstrip line" is indefinite because it is misdescriptive. Figure 2 shows that there is **only one opening** (32) that is located **next** to the through hole (30). This opening (32) **is not aligned** with the through hole (30) as recited.

Regarding claim 9, the recitation " wherein said opening aligned with the microstrip line is arranged such that...said microstrip line" has the same 112, 2nd problem of claim 2.

Regarding claim 10, the recitation "openings" has the same 112, 2nd problem of claims 3 and 8.

Regarding claim 16, the recitation "wherein said omitted portion aligned with...said microstrip line" has the same 112, 2nd problem of claims 2 and 9.

Regarding claim 17, the recitations "omitted portions" and "openings" and "two conductor layers" have the 112, 2nd problem as mentioned above.

Claims 5-7, 11-13, 15 and 19-21 are indefinite because of the technical deficiencies of claim 1, 8 and 14.

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-21, insofar as understood, are rejected under 35 U.S.C. 102(b) as being anticipated by Mandai et al. (US Pat. 5,227,739).

Regarding claim 1, figure 4 of Mandai shows a resonator comprising: a multi-layer substrate having an upper and lower surface, and including at least two grounding conductor layers (3,5,7) and a plurality of dielectric layers (2a-2g), one of the at least two grounding conductor layers (3) being disposed on the lower surface of the multi-layer substrate; a strip line (4) disposed between the at least two grounding conductor layers (3,5); a microstrip line (9) disposed on the upper surface of said multi-layer substrate; and a through hole (V1) formed in said dielectric layers (2e, 2f, 2g) to connect said strip line (4) to said microstrip line (9); wherein portions (V1) of the one of the at least two grounding conductor layers (7) that is closest to said microstrip line (9) are omitted. The omitted portions (V1) are "aligned" with the through hole and the microstrip (9). Note that there is a plurality of omitted portions and through holes (V1). The through hole is inside omitted portion thus; the through hole is aligned with the omitted portion (opening).

Regarding claims 2, 3, 4 and 5 the portion of said one of the at least two conductor layers that is omitted (7) is disposed "inside" said multi-layer substrate and is arranged such that said grounding conductor layer disposed on the lower surface of said multi-layer substrate faces said microstrip line (9). The omitted portion defines the opening in the one of the least two conductor layers and the shape of the hole is rectangular. The strip line (4) has an U-shaped configuration.

Regarding claims 6 and 7, the strip line is (4) and the micro strip line is (9).

Regarding claim 8, 9, 10, 11, 12 and 13, figure 4 of Mandai shows a resonator comprising: a multi-layer substrate having an upper and lower surface, and including at least two grounding conductor layers (3,5,7) and a plurality of dielectric layers (2a-2g), one of the at least two grounding conductor layers (3,5) being disposed on the lower surface of the multi-layer substrate, and one of the at least two conductor layers (5,7) that is closest to said microstrip line has openings (V1, V2) formed therein; a strip line (4) disposed between the at least two grounding conductor layers (3,5); a microstrip line (9) disposed on the upper surface of said multi-layer substrate; and a through hole (V1) formed in said dielectric layers to connect said strip line to said microstrip line ; wherein the openings (V1) are "aligned" with the through hole and the microstrip (9). Note that there is a plurality of omitted portions (openings) and through

holes (V1). The through hole is inside omitted portion, thus the through hole is aligned with the omitted portion (opening).
The grounding conductor layer (3) faces the strip line (4). The opening (V1) has a rectangular shape and the strip line (4) has an U- shaped configuration. The resonator comprises only one strip line (4). The resonator comprises a microstrip line (9).

Regarding claims 14 and 15, figure 4 of Mandai shows a voltage controlled oscillator comprising: a resonator including: a multi-layer substrate having an upper and lower surface, and including at which include at least two grounding conductor layers (3,5,7) and a plurality of dielectric layers (2a-2g), one of the at least two grounding conductor *layers being disposed on* the lower surface of the multi-layer substrate; a strip line (4) disposed between the at least two grounding conductor layers; a microstrip line (9) disposed on the upper surface of said multi-layer substrate; and a through hole (V1) formed in said dielectric layers to connect said strip line to said microstrip line; wherein portions (V1) of the one of the at least two conductor layers (7) that is closest to said microstrip line (9) are omitted. The omitted portions (V1) are "aligned" with the through hole and the microstrip (9). Note that there is a plurality of omitted portions and through holes (V1). The through hole is inside omitted portion, thus the through hole is aligned with the omitted portion (opening). A plurality of electronic component elements disposed on the upper surface (2g) of the multi-layer substrate and arranged to define a circuit and inherently the plurality of the electronic component elements and the resonator are electrically connected to each other.

Regarding claim 16, said omitted portion (V1) aligned with the microstrip line (9) is arranged "such that said grounding conductor layer (3) disposed on the lower surface of said multi-layer substrate faces said microstrip line (9)".

Regarding claims 17, the omitted portions (V1) define openings in said one of the at least two grounding conductor layers (3, 5, 7).

Regarding claims 18 and 19, the strip line (4) has an U shape and the openings (V1) have a substantially rectangular shape or square shape.

Regarding claims 20 and 21, the voltage-controlled oscillator comprises only one micro-strip line (9) or only one strip line (4).

Response to arguments

In the Remarks, the Applicant argues that Mandai et al. does not teach or suggest the feature of "one omitted portion is aligned with the through hole and another portion is aligned with the microstrip line". This is not true. Figure 4 of Mandai shows a voltage-controlled oscillator (resonator) comprising a microstrip line (9), a strip line (4) and a plurality of omitted portions (openings) (V1). The omitted portions are also through holes. The through holes connect the microstrip line (9) to the strip line (4). Thus, the omitted portions are aligned with the through hole and the microstrip line. The Applicant is reminded that by definition the microstrip line is a microwave transmission component in which **a single conductor** is supported above a ground plane. The microstrip is also called **strip line**.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Hiep Nguyen whose telephone number is (703) 305-0127. The examiner can normally be reached on Monday to Friday from 7:30 A.M.to 4:00 P.M.. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (703) 308-4876. The fax phone number for this Group is (703) 308-66251.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

Hiep Nguyen
09-24-03

TUAN T. LAM
PRIMARY EXAMINER